
Roll No :

KLNCIT	CENTRALIZED INTERNAL TEST QUESTION	Format No. :ACD11A-II Issue No. :01 Rev No. :00

Subject Code/Subject Name: CS6303-Computer Architecture **CIT No. : II**
Year and Branch : IIyr / Common to CSE &IT **Total marks: 50**
Date : 20.09.2017 **Duration : 1 hour 30mins**

I. Course outcomes, Question Number, Marks

COs	CO1	CO2	CO3	CO4	CO5
Q. Nos			1-5,11a/11b	6-10, 12a / 12b	
Marks (Max)			25	25	

II. Knowledge skill outcomes

Level	Remember (K1)	Understand (K2)	Apply (K3)	Analysis (K4)	Evaluate (K5)	Create (K6)
Q. Nos	1,3,4,6-10	5, 11(a)/11(b), 12a(i)/12b(i)	2			
Marks (Max)	16	32	2			

PART – A **10 × 2 = 20 Marks**

Answer all the questions

1. What do you mean by pipeline bubble? K1

A stall initiated in order to resolve a hazard.

2. Assume all variables are in memory and are addressable offsets from $t0:

```
lw $t1, 0($t0)
lw $t2, 4($t0)
add $t3, $t1,$t2
sw $t3, 12($t0)
lw $t4, 8($t0)
add $t5, $t1,$t4
sw $t5, 16($t0)
```

Reorder the instructions to avoid any pipeline stalls. (K3)

```
lw $t1, 0($t0)
lw $t2, 4($t0)
lw $t4, 8($t0)
add $t3, $t1,$t2
sw $t3, 12($t0)
add $t5, $t1,$t4
sw $t5, 16($t0)
```

3. What is delayed branch? (K1)

The delayed branch always executes the next sequential instruction, with the branch taking place *after* that one instruction delay. It is hidden from the MIPS assembly language programmer because the assembler can automatically arrange the instructions to get the branch behavior desired by the programmer.

4. Why forwarding or bypassing is necessary? (K1)

forwarding Also called **bypassing**. A method of resolving a data hazard by retrieving the missing data element from internal buffers rather than waiting for it to arrive from programmer visible registers or memory.

5. How a 2-bit branch prediction scheme is better than 1-bit branch prediction scheme? Compare your result. (K2)

By using 2 bits rather than 1, a branch that strongly favors taken or not taken—as many branches do—will be mispredicted only once. The 2 bits are used to encode the four states in the system. The 2-bit scheme is a general instance of a counter-based predictor, which is incremented when the prediction is accurate and decremented otherwise, and uses the mid-point of its range as the division between taken and not taken.

6. What are the primary methods for increasing the instruction level parallelism (ILP)? (K1)

First is increasing the depth of the pipeline to overlap more instructions.

Another approach is to replicate the internal components of the computer so that it can launch multiple instructions in every pipeline stage.

7. Define speculation. (K1)

Speculation An approach whereby the compiler or processor guesses the outcome of an instruction to remove it as a dependence in executing other instructions.

8. What is Very Long Instruction Word (VLIW)? (K1)

Very Long Instruction Word (VLIW) A style of instruction set architecture that launches many operations that are defined to be independent in a single wide instruction, typically with many separate opcode fields.

9. What are NUMA and SMP? (K1)

A shared memory multiprocessor (SMP) is one that offers the programmer a single physical address space across all processors, which is nearly always the case for multicore chips although a more accurate term would have been shared-address multiprocessor.

Nonuniform memory access (NUMA) A type of single address space multiprocessor in which some memory accesses are much faster than others depending on which processor asks for which word.

10. Brief about multithreading. (K1)

Hardware multithreading Increasing utilization of a processor by switching to another thread when one thread is stalled.

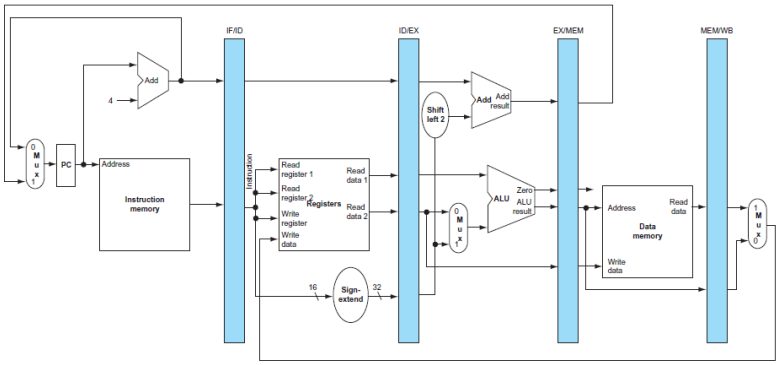
Fine-grained multithreading A version of hardware multithreading that implies switching between threads after every instruction.

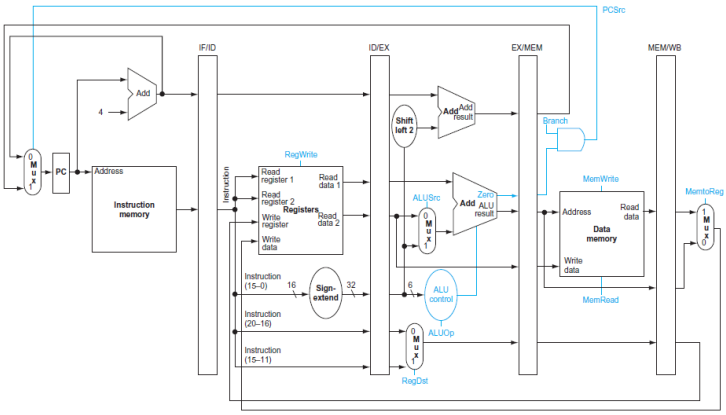
Coarse-grained multithreading A version of hardware multithreading that implies switching between threads only after significant events, such as a last-level cache miss.

PART – B

2 × 15 = 30 Marks

11. (a) Explain in detail about pipelined datapath and control. (K2)





(OR)

(b) Explain in detail about how exceptions are handled in MIPS architecture. (K2)

Type of event	From where?	MIPS terminology
I/O device request	External	Interrupt
Invoke the operating system from user program	Internal	Exception
Arithmetic overflow	Internal	Exception
Using an undefined instruction	Internal	Exception
Hardware malfunctions	Either	Exception or interrupt

Exception type	Exception vector address (in hex)
Undefined instruction	$8000\ 0000_{hex}$
Arithmetic overflow	$8000\ 0180_{hex}$

Status Register
EPC
Vectored Interrupt

12. (a) Explain in detail about Flynn's classification. (K2)
SISD
SIMD
MISD
MIMD

(OR)

(b) Explain Instruction level parallelism. State the challenges of parallel processing. (K2)
ILP
Static multiple issues
Dynamic multiple issues
Issue slots
Speculation
Issue packet
VLIW
Example
Challenges:

The fist reason is that you *must* get better performance or better energy efficiency from a parallel processing program on a multiprocessor
Speed-up challenge
Strong scaling
Weak scaling
Load balancing

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